Design and Simulation of a LDO voltage regulator

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***Abstract*—This paper gives a short introduction into basic linear voltage regulator operation, and focuses then on low-dropout (LDO) regulators and the main pitfall in application. A simulation utilizing LTSpice is performed to analyze the stability of the closed feedback loop. The simulation is briefly compared with measurement results based on a breadboard layout of the circuit.**

***Index Terms*—Power electronics, DC-DC power converters, Circuit simulation, Circuit stability.**

I. Introduction

WHILE being available for more than 30 years, one of the most often used devices for DC-DC-voltage conversion is still the linear voltage regulator.

All linear voltage regulators reduce an input voltage to a constant output voltage across a load. They are not capable to increase the voltage, like switchmode power supplies and charge pumps. In the past years, a lot of so called low-dropout devices found their way on the market, reducing the needed voltage difference between input and output from volts down to millivolts, at the cost of the problem of regulation stability.

A. Basic linear regulator operation

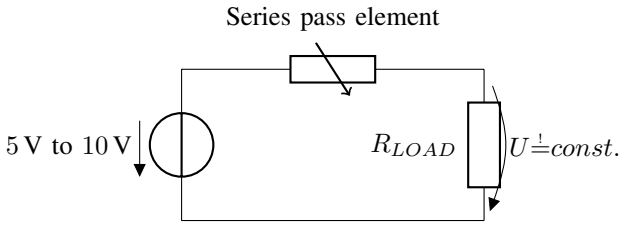

Figure 1. Basic idea behind linear voltage regulators

The basic idea behind linear voltage regulators (as shown in figure 1), is to adjust the resistance of a series pass element in such a way, that the voltage across the load remains constant. The input voltage may be varying (think of battery or solar panels), the load itself may not be constant, as often devices show a large difference in supply current between standby and actual operation. In all these cases, the output voltage must remain constant.

II. Low-dropout regulator

The basic circuit of a LDO regulator is shown in figure 2. In modern devices a PMOS transistor is used as series pass element, as it has several advantages over PNP transistors [1], [2].

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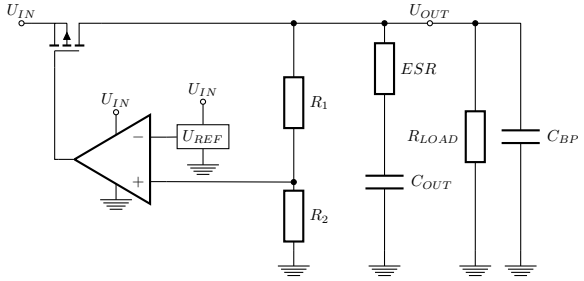

Figure 2. Basic LDO circuit

As it can be seen, a LDO utilizes a closed feedback loop to regulate the output voltage U_{OUT}. An error amplifier regulates the resistance of the PMOS transistor, so that the output voltage of the voltage divider network formed by R_1 and R_2 matches that of a built in voltage reference.

As the PMOS transistor can easily be driven into saturation, the minimum dropout voltage is given by the load current and the $R_{DS_{ON}}$ of the transistor (1).

$$U_{DO} \approx I_{LOAD} \cdot R_{DS_{ON}} \tag{1}$$

The voltage reference is a critical part, as the output voltage drift and accuracy can never be better than the one of the reference. Because of that a bandgap reference is often used, as they have very low temperature coefficients. The design of a bandgap voltage reference can be tricky and is discussed in [3].

As for any closed feedback loop, the stability criterion, as dictated by Nyquist, must be met. In practice the criteria says, that the phase margin at unity gain of the open loop must be bigger than $45°$ to indicate stability.

The stability of a LDO is one of the main pitfalls in the application of them. In former times the designer always tried to use a output capacitor with as low equivalent series resistance (ESR) as possible. With the upcoming multilayer ceramic capacitors (MLCC) with very high capacity and very low ESR this can be a problem, as the stability of a LDO requires a minimum ESR.

III. Stability analysis

There are different approaches to stability analysis of the LDO circuit. One is a pole-zero analysis as described in [1], [4]. Three poles and one zero can be identified in the basic circuit. The first pole arises from the PMOS transistors output resistance and the output capacitance (2), the approximation is given in [4], λ is the channel length modulation of the PMOS transistor. The second pole is formed by the ESR and the bypass capacitor (3). The equivalent output resistance of the error amplifier and the equivalent capacitance of the PMOS

form the third pole (4). The zero is formed by the ESR and the output capacitor (5).

$$p_1 \approx \frac{1}{2\pi \cdot R_{PMOS} \cdot C_{OUT}} \approx \frac{\lambda \cdot I_{LOAD}}{2\pi \cdot C_{OUT}} \tag{2}$$

$$p_2 \approx \frac{1}{2\pi \cdot ESR \cdot C_{BP}} \tag{3}$$

$$p_3 \approx \frac{1}{2\pi \cdot R_{OPA} \cdot C_{PMOS}} \tag{4}$$

$$z_1 \approx \frac{1}{2\pi \cdot ESR \cdot C_{OUT}} \tag{5}$$

For a complete analysis the loop gains must be determined. In this circuit there are three different gains to be considered. The first one is the gain of the feedback resistor network (G_{FB}), the second is the DC gain of the error amplifier (G_{OPA}) and the third gain is from the PMOS transistor (G_{PMOS}). The complete expression to determine the open-loop gain is given in (6).

$$G(s) = G_{FB} \cdot G_{OPA} \cdot G_{PMOS} \cdot \frac{1 + \frac{s}{2\pi z_1}}{\left(1 + \frac{s}{2\pi p_1}\right) \cdot \left(1 + \frac{s}{2\pi p_2}\right) \cdot \left(1 + \frac{s}{2\pi p_3}\right)} \tag{6}$$

The problem with this kind of analysis is, that getting all the parameters can be troublesome because most of them are not specified in datasheets. For actual designers of a complete LDO, some of these values are design parameters like the equivalent output resistance of the error amplifier.

IV. Stability analysis using LTSpice IV

Another way to perform a stability analysis is using one of the many Spice circuit simulators. For this research LTSpice IV[1] was used.

There are two basic approaches to stability analysis when using Spice. One is doing a transient analysis and observe the output voltage to see if it is stable. Another way is to simulate the open-loop gain and confirm the stability using the criteria mentioned above.

A. Transient analysis for stability

The easiest way is to set up the circuit and do a transient analysis. One thing which is important to get reliable results is to select the DC-voltage startup. This will basically start all DC voltages from 0 V and ramp them up to their set values. This will help greatly to reveal instability. Also the simulation time should not set to be too short, sometimes the instability appears after some milliseconds and not right at the beginning. This problem limits the trust in this method. You can never be really sure if your simulation time was long enough or not.

To demonstrate this a basic circuit was simulated using different output capacitor ESR values, the capacitance was an unchanged value of 10 µF. The first simulation was using a MLCC capacitor from TDK with an ESR of 0.001 Ω. As can be seen in figure 3 the simulation without startup just starts to oscillate at the end of the simulation time of 50 ms, the simulation with startup (dotted line) shows a peak at the start but then oscillates right after that peak.

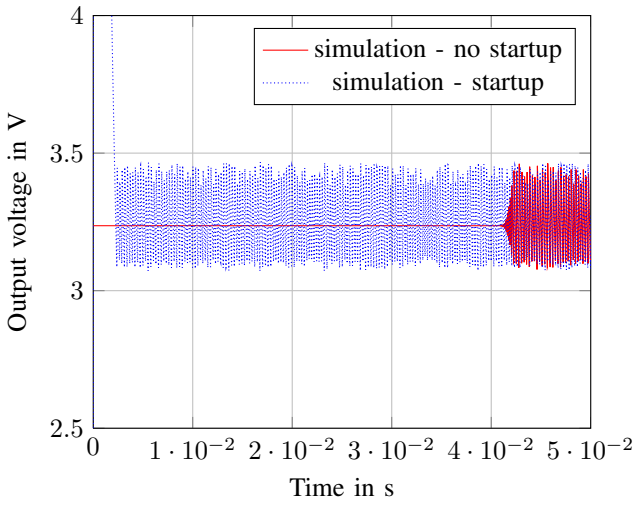

Figure 3. Transient analysis - MLCC with 10 µF and 0.001 Ω ESR, Y-Axis truncated to show oscillation

The second simulation uses a tantalum capacitor from KEMET with an ESR of 0.3 Ω which leads to the results in figure 4. In this case, the simulation without startup option doesn't lead to any oscillation within 50 ms, and the simulation with startup shows only a slight oscillation at the beginning before getting stable. But this still indicates that there might be stability issues in this configuration.

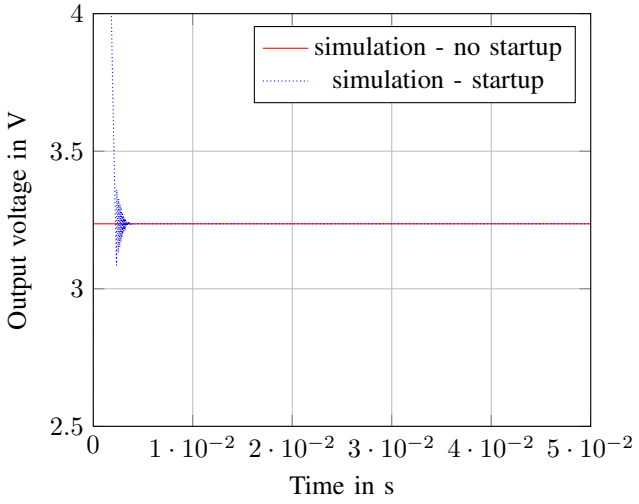

Figure 4. Transient analysis - Tantalum with 10 µF and 0.3 Ω ESR, Y-Axis truncated to show oscillation

The last simulation used an aluminium electrolytic capacitor from Nichicon with an ESR of 2.8 Ω. As it turns out, there is no oscillation in either case (see figure 5).

B. Open-loop gain analysis with LTSpice

Less intuitive but giving good information on stability is to determine the open-loop gain of the circuit with LTSpice.

[1] available from Linear Technology: http://ltspice.linear.com/software/LTspiceIV.exe

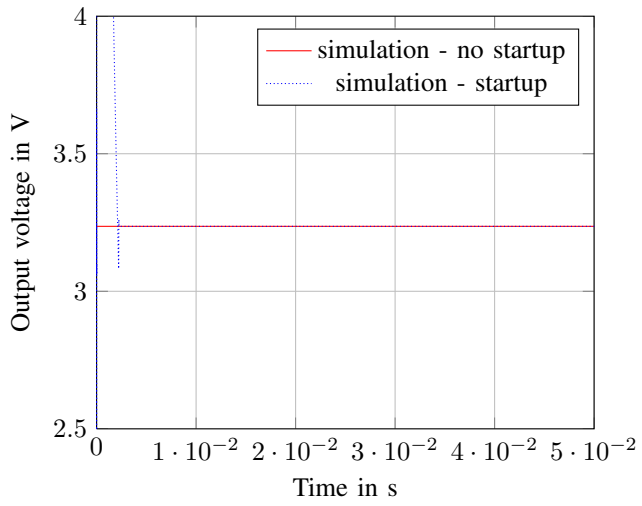

Figure 5. Transient analysis - Aluminium electrolytic with 10 µF and 2.8 Ω ESR, Y-Axis truncated to show oscillation

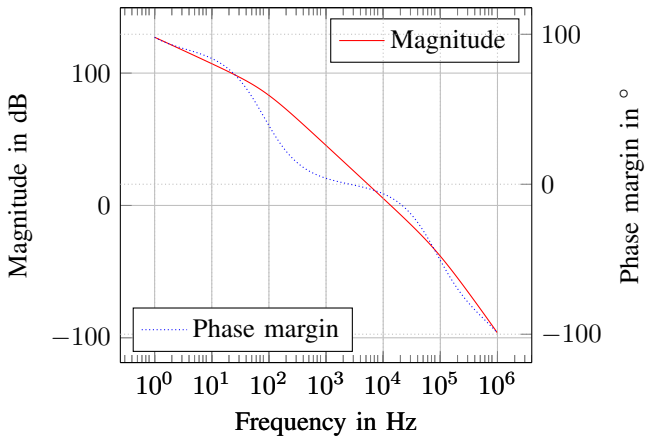

Figure 6. Bode plot - MLCC with 10 µF and 0.001 Ω ESR

The problem arising here, is that cutting the closed loop open, will result in a greatly different response of the circuit, making the result virtually worthless. Normally a impedance matching has to be performed to compensate for opening the loop. This needs careful consideration on where to cut and how to compensate.

Utilizing the double-injection technique described in [5] it is possible to easily get a simulation result for the open loop gain of the feedback system. Dr. Frank Wiedmann published a complete implementation[2] of this method for usage in LTSpice.

Another possibilty is the usage of the so called General Feedback Theorem (GFT) described in [6], which shall be mentioned here only for completeness.

For this research the double-injection technique was used. The loop-gain-probe was inserted into the circuit and the analysis was switched to an AC analysis. It is important to enable the saving of subcircuits voltages and currents, as they are needed for the calculation of the open-loop gain.

Performing this technique on the circuits with the different capacitors leads to the graphics 6,7 and 8. It can be seen, that the phase margin in the first case is around $-8.8°$ and thus indicates an unstable system, which could be seen in the transient analysis as well. The medium ESR capacitor leads to a phase margin of $5.5°$ which is still not enough to be considered really stable, which could also be observed as ringing in the transient analysis using startup. With the third capacitor the phase margin increases to $59.4°$ and can be considered stable.

V. Comparison with measurement results

The simulated circuit was built on a breadboard as an easy setup. As voltage sources standard AA-size batteries were used. The simulation values and components are equal to those of the breadboard design, with one difference concerning

[2]available online: http://sites.google.com/site/frankwiedmann/loopgain

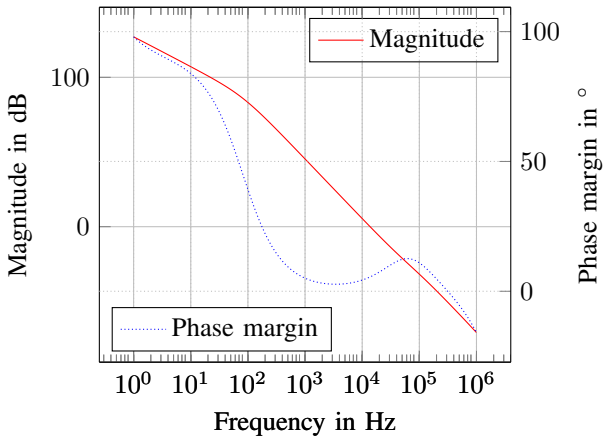

Figure 7. Bode plot - Tantalum with 10 µF and 0.3 Ω ESR

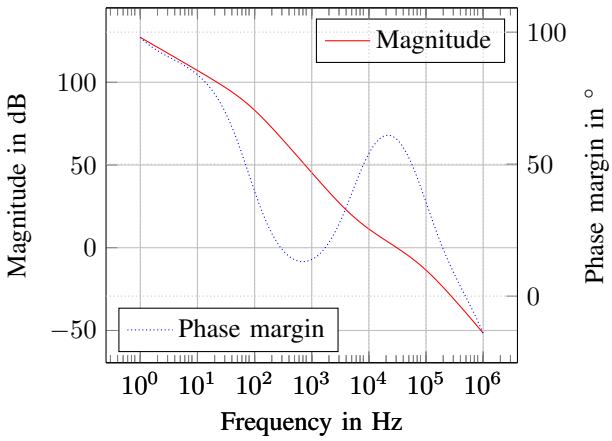

Figure 8. Bode plot - Aluminium electrolytic with 10 µF and 2.8 Ω ESR

the output capacitor. The only available capacitor was an electrolytic type with not specified ESR value.

To check system stability the output capacitor was removed completely and another transient simulation was done to compare the waveform with a measured on an oscilloscope.

Using an $10\,\mu F$ output capacitor, there was no oscillation measurable. The output voltage could be measured as $3.22\,V \pm 0.04\,V$. The simulated value is $3.236\,V$ which is a deviation of only $0.5\,\%$.

Removing the capacitor there is an oscillation appearing, the transient simulation also shows an oscillation if the DC voltage startup is selected. Both of the waveforms are plotted in one diagram in figure 9. The measurement was taken with an Rigol DS1102E digital storage oscilloscope.

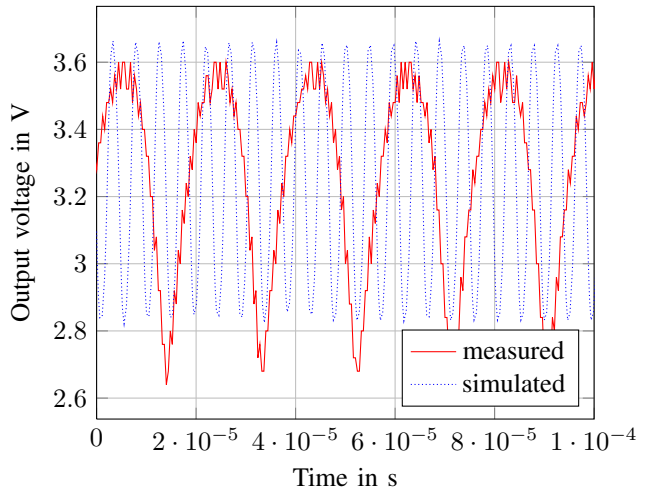

Figure 9. Transient waveforms of measured and simulated data without output capacitor

As it can be observed, the simulation and the measurement differ greatly. The amplitude of the oscillation is off by $-0.1\,V$ which is approximately $-11\,\%$. The frequency of the measured oscillation is $52\,kHz$ while the simulation shows around $200\,kHz$. Which is a difference of $285\,\%$. In the simulation the loading of the probe was applied ($1\,M\Omega$ and $120\,pF$ in parallel to the load resistor).

A reason for this difference might be due to the parasitic capacitance which were neglected during simulation. As well as the breadboard design is not suitable for high frequency application and is susceptive for interferences.

Another reason might be the relatively old spice models of the used components, which date back to 1990, and thus may not provide the needed precision especially if oscillations are occurring.

VI. Conclusion

In this paper the basic design of a LDO voltage regulator using a PMOS transistor as series pass element was presented. An analytical stability analysis of a design based on supplied components is very hard to achieve as several parameters are needed, which are not available from part manufacturers.

To perform a stability analysis the LTSpice simulator was used performing transient and AC analysis. For AC analysis the double-injection technique was applied. Both methods showed instabilities, but the transient analysis can give misleading results if DC-voltage startup is not selected. Generally the double-injection technique giving the open-loop gain gives a better estimate for stability as the phase margin can be obtained.

Comparison with measurements taken on a breadboard layout showed, that the stable results of the simulation are very good with an error of only $0.5\,\%$. The result of an unstable circuit differed greatly from the measured values, the source of this error may be not precise models or the fact, that parasitic capacitances were neglected in the simulation.

References

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Appendix
Availability of Simulation Data

All data used and the simulation circuit will be made available on http://www.arsenal-of-wisdom.org